(d) high resistance controllable current leakage imperfect isolating means connecting said bit line to said sense nodes for receiving an enabling voltage for causing current leakage therethrough between said sense nodes and the bit line while maintaining high resistance,

(e) means for applying said enabling voltage for causing effective current to leak through the imperfect isolating means,

[(e)] (f) means for enabling said sense amplifier and establishing full predetermined logic levels across said sense nodes,

cont. C1

[(f)] (g) means for disabling said imperfect isolating means and thereby removing isolation between said sense nodes and the bit line,

whereby current passing through the sense amplifier to said sense nodes is enabled to charge said bit line capacitance through said imperfect isolating means to a predetermined logic voltage level.

REMARKS

Claim 1 has been further amended to more clearly described the features of the present invention.

Entry of the preliminary amendments and examination of the application is respectfully requested.

To the extent necessary, applicant's petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account

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